REMARKS

Claims 1-30 are pending in the present application. Claims 1-27 were rejected and Claims 28-30 were objected to, but have allowable subject matter. Applicants traverse the objected to and rejected claims. Claims 5, 13-16, and 28 are cancelled. Claims 1-3, 10-12, 14-15, 17-18, 20, and 22 were rejected under 35 USC 102(e) as being anticipated by US Patent 6,829,751 (hereinafter "Shen"). Claims 4-9, 13, 16, 21 and 23-27 were rejected under 35 USC 103(a) as being obvious in view of Shen combined with US Patent 6,405,335 (hereinafter "Whetsel").

Claim 1 has been amended to include among other features: configuring the configurable logic fabric for a test comprising, forming a scan chain in the configurable logic fabric; providing scan data from at least a portion of the scan chain to the embedded device; performing the test on the embedded device ; and at least another portion of the scan chain receiving test results from the embedded device. The Examiner conceded that Shen does not have all these features, but the Examiner argues that Shen in combination with Whetsel includes the scan collector receiving the test results. The Applicants disagree.

Whetsel in FIG. 3 and claim 1 describe a scan distributor 300 having a serial input from a bond pad 302 and connected to ten parallel scan paths 324-342. The ten parallel scan paths 324-342 are connected to a scan collector circuit 344 [col. 4, lines 7-16]. FIG. 7 shows an integrated circuit (IC) 700 with a complex core circuit 704 [col. 8, lines 29-38]. FIG. 8 shows that there is one scan distributor and scan collector arrangement 800/844 for testing the functional part of the IC and another scan distributor and scan collector arrangement 900/944 for testing the embedded core 704 [col. 8, line 45 – col. 9 line 40]. As seen from FIG. 8 the scan distributor, ten parallel scan paths and scan collector are embedded in and part of the complex core circuit 704.

Shen in FIG. 3 shows a segmented scan chain 162 in FPGA core 116 [col. 4, lines 12-23]. FIG. 5 shows that FPGA core 116 can be used to bridge signals between different modules 202a-202n [col. 5, lines 1-4] and to drive signals to test the specific module [c0l. 6, lines 45-56]. Thus in Shen the scan chain is part of the FPGA core

which is then used to test the embedded device and not part of the embedded device.

Combining Whetsel, having an embedded device with its own embedded hardwire scan chain, in the IC 102 of Shen would render the scan chain in FIG. 3 of FPGA core 116 unnecessary to test the embedded device (i.e., module 202a of FIG. 5). Thus the combination would render Shen unsatisfactory for its intended purpose. For this reason alone, the rejection of claim 1 should be withdrawn.

In addition, there is no disclosure or teaching in Shen to embed a complex module that requires the more complicated multiple parallel scan paths and scan distributor and collector circuits of Whetsel. Indeed, Shen teaches away from the multiple parallel scan paths by segmenting the serial scan chain to speed up data collection [col. 4, lines 6-11]. For these reasons alone, the rejection of claim 1 should be withdrawn.

For the above reasons claim 1 should be allowable. Claims 2-9 being dependent upon claim 1 should be allowable for at least the reasons claim 1 is allowable.

Claim 10 has been amended to include among other features: configuring the IC for test, comprising forming a scan chain in the configurable logic fabric, wherein the scan chain receives the test data; transferring the test data from the scan chain to a multiplexer, wherein the multiplexer is a part of interfacing circuitry, and wherein the interfacing circuitry couples the processor to the configurable logic fabric; and transferring the test data from the multiplexer to the processor. For at least the reasons claim 1 is allowable claim 10 should be allowable.

Claims 11-12 being dependent upon claim 10 should be allowable for at least the reasons claim 10 is allowable.

Claim 17 has been amended to include among other features: a scan chain formed in the programmable logic fabric for testing the fixed logic circuit, wherein at least some input test data is sent from the scan chain to the fixed logic circuit via a first multiplexer of the plurality of multiplexers and at least some test results from the fixed logic circuit are received by the scan chain via a second multiplexer of the plurality of multiplexers. Neither Shen nor Whetsel or any combination thereof, discloses or suggests these features. Thus claim 17 should be allowable.

Claims 18-26 being dependent upon claim 17 should be allowable for at least the reasons claim 17 is allowable.

Claim 27 has been amended to include the limitations of claim 28 and should now be allowable.

Claims 29-30 being dependent upon claim 27 should be allowable for at least the reasons claim 27 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 09, 2006.

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